What is Claimed is:

1. A bonding pad for an integrated circuit comprising:

first and second spaced apart conductive patterns and a dielectric layer therebetween; and

a closed conductive pattern in the dielectric layer, electrically connecting the first and second spaced apart conductive patterns, the closed conductive pattern enclosing an inner portion of the dielectric layer, and being enclosed by an outer portion of the dielectric layer.

2. A bonding pad according to Claim 1 wherein the closed conductive pattern is at least one of a circular, elliptical and polygonal conductive pattern.

3. A bonding pad according to Claim 1 further comprising a second closed conductive pattern in the inner portion of the dielectric layer, electrically connecting the first and second spaced apart conductive patterns.

4. A bonding pad according to Claim 1 further comprising an open conductive pattern in the inner portion of the dielectric layer, electrically connecting the first and second spaced apart conductive patterns.

5. A bonding pad according to Claim 1 further comprising:

a third conductive pattern that is spaced apart from the second conductive pattern;

a second dielectric layer between the second and third conductive patterns; and

a fourth conductive pattern in the dielectric layer, electrically connecting the second and third spaced apart conductive patterns.

6. A bonding pad according to Claim 5 wherein the fourth conductive pattern comprises a second closed conductive pattern in the second dielectric layer, electrically connecting the second and third spaced apart conductive patterns, the second closed conductive pattern enclosing a second inner portion of the second

dielectric layer, and being enclosed by a second outer portion of the second dielectric layer.

7. A bonding pad according to Claim 6 wherein the second and third conductive patterns are congruent to one another and wherein the closed conductive pattern and the second closed conductive pattern are of same shape but of different sizes.

8. A bonding pad according to Claim 6 wherein the closed conductive pattern is an elliptical conductive pattern and wherein the second closed conductive pattern is a polygonal closed conductive pattern.

9. A bonding pad for an integrated circuit comprising:

first and second spaced apart conductive patterns and a dielectric layer therebetween, the dielectric layer including a closed via therein that extends between the first and second spaced apart conductive patterns, the closed via enclosing an inner portion of the dielectric layer, and being enclosed by an outer portion of the dielectric layer; and

a closed conductive pattern in the closed via, electrically connecting the first and second spaced apart conductive patterns.

10. A bonding pad according to Claim 9 wherein the closed conductive pattern fills the closed via.

11. A bonding pad according to Claim 9 wherein the closed via is at least one of a circular, elliptical and polygonal via.

12. A bonding pad according to Claim 9 further comprising a second closed via in the inner portion of the dielectric layer; and

a second closed conductive pattern in the second closed via, electrically connecting the first and second spaced apart conductive patterns.

13. A bonding pad according to Claim 9 further comprising:

an open via in the inner portion of the dielectric layer; and

an open conductive pattern in the open via, electrically connecting the first and second spaced apart conductive patterns.

14. A bonding pad according to Claim 9 further comprising:

a third conductive pattern that is spaced apart from the second conductive pattern;

a second dielectric layer between the second and third conductive patterns, the second dielectric layer including a second via therein that extends between the second and third spaced apart conductive patterns; and

a fourth conductive pattern in the second via, electrically connecting the second and third spaced apart conductive patterns.

15. A bonding pad according to Claim 14:

wherein the second via comprises a second closed via in the second dielectric layer that encloses an inner portion of the second dielectric layer, and is enclosed by a second outer portion of the second dielectric layer; and

wherein the fourth conductive pattern is a second closed conductive pattern in the second via.

16. A bonding pad according to Claim 15 wherein the second and third conductive patterns are congruent to one another and wherein the closed conductive pattern and the second closed conductive pattern are of same shape but of different sizes.

17. A bonding pad according to Claim 15 wherein the closed conductive pattern is an elliptical conductive pattern and wherein the second closed conductive pattern is a polygonal closed conductive pattern.

18. An integrated circuit comprising:

an integrated circuit substrate; and

a bonding pad on the integrated circuit substrate, the bonding pad comprising:

first and second spaced apart conductive patterns and a dielectric layer therebetween, on the integrated circuit substrate; and

a closed conductive pattern in the dielectric layer, electrically connecting the first and second spaced apart conductive patterns.

19. An integrated circuit according to Claim 18 wherein the closed conductive pattern is at least one of a circular, elliptical and polygonal conductive pattern.

20. An integrated circuit according to Claim 18 further comprising a second closed conductive pattern within the closed conductive pattern, electrically connecting the first and second spaced apart conductive patterns.

21. An integrated circuit according to Claim 18 further comprising an open conductive pattern in the dielectric layer, electrically connecting the first and second spaced apart conductive patterns.

22. An integrated circuit according to Claim 18 further comprising:

a third conductive pattern that is spaced apart from the second conductive pattern;

a second dielectric layer between the second and third conductive patterns; and

a fourth conductive pattern in the dielectric layer, electrically connecting the second and third spaced apart conductive patterns.

23. An integrated circuit according to Claim 22 wherein the fourth conductive pattern comprises a second closed conductive pattern in the second dielectric layer, electrically connecting the second and third spaced apart conductive patterns.

24. An integrated circuit according to Claim 23 wherein the second and third conductive patterns are congruent to one another and wherein the closed

conductive pattern and the second closed conductive pattern are of same shape but of different sizes.

25. An integrated circuit according to Claim 23 wherein the closed conductive pattern is an elliptical conductive pattern and wherein the second closed conductive pattern is a polygonal closed conductive pattern.

26. An integrated circuit comprising:

an integrated circuit substrate; and

a bonding pad on the integrated circuit substrate, the bonding pad comprising:

first and second spaced apart conductive patterns and a dielectric layer therebetween on the integrated circuit substrate, the dielectric layer including a closed via therein that extends between the first and second spaced apart conductive patterns; and

a closed conductive pattern in the closed via, electrically connecting the first and second spaced apart conductive patterns.

27. An integrated circuit according to Claim 26 wherein the closed conductive pattern fills the closed via.

28. An integrated circuit according to Claim 26 wherein the closed via is at least one of a circular, elliptical and polygonal via.

29. An integrated circuit according to Claim 26 further comprising:

a second closed via in the dielectric layer, within the closed via; and

a second closed conductive pattern in the second closed via, electrically connecting the first and second spaced apart conductive patterns.

30. An integrated circuit according to Claim 26 further comprising an open via in the dielectric layer; and

an open conductive pattern in the open via, electrically connecting the first and second spaced apart conductive patterns.

31. An integrated circuit according to Claim 26 further comprising:

a third conductive pattern that is spaced apart from the second conductive pattern;

a second dielectric layer between the second and third conductive patterns, the second dielectric layer including a second via therein that extends between the second and third spaced apart conductive patterns; and

a fourth conductive pattern in the second via, electrically connecting the second and third spaced apart conductive patterns.

32. An integrated circuit according to Claim 31:

wherein the second via comprises a second closed via in the second dielectric layer; and

wherein the fourth conductive pattern is a second closed conductive pattern in the second via.

33. An integrated circuit according to Claim 32 wherein the second and third conductive patterns are congruent to one another and wherein the closed conductive pattern and the second closed conductive pattern are of same shape but of different sizes.

34. An integrated circuit according to Claim 32 wherein the closed conductive pattern is an elliptical conductive pattern and wherein the second closed conductive pattern is a polygonal closed conductive pattern.

35. A method of forming bonding pad for an integrated circuit comprising the steps of:

forming a dielectric layer on an integrated circuit substrate, the dielectric layer including a closed via therein that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer; and

forming a conductive pattern in the closed via and on the dielectric layer opposite the substrate.

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36. A method according to Claim 35 wherein the step of forming a conductive pattern comprises the step of forming a conductive pattern filling the closed via and on the dielectric layer opposite the substrate.

37. A method according to Claim 35 wherein the steps of forming a dielectric layer and forming a conductive pattern are repeatedly performed to form a multilayer bonding pad on the integrated circuit substrate.

38. A method according to Claim 35 wherein the closed via is at least one of a circular, elliptical and polygonal via.

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39. A method according to Claim 35:

wherein the step of forming a dielectric layer comprises the step of forming a dielectric layer on an integrated circuit substrate, the dielectric layer including the closed via and an open via therein; and

wherein the step of forming a conductive pattern comprises the step of forming a conductive pattern in the closed via, in the open via and on the dielectric layer opposite the substrate.

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